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Characterization of an Integrated GaN Driver for Power Switching Applications

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Keywords

«Gallium Nitride (GaN)», «Gate Driver», «Device characterisation».

Abstract

Modern GaN-HEMTs require appropriate driving circuits to enable fast switching. Thus, monolithic integration of power switches and gate drivers is necessary. Therefore, this paper demonstrates a GaN driver to control a GaN power switch. Besides static and pulsed characterization, the driver's performance is validated through continuous switching tests, demonstrating effective operation with turn-on and turn-off times of an emulated load of 1.68 ns and 1.84 ns, respectively.

Introduction

Gallium Nitride High-Electron-Mobility Transistors (GaN-HEMTs) are attractive candidates for highly efficient and high-density power electronic converters. Besides low conduction losses resulting from small on-state resistance, high-density converters must also benefit from low switching losses to allow pushing the switching frequency. Increasing the switching frequency shrinks the size of passives which then raises the power density [1]. Fast switching transitions not only require optimized layouts for the commutation cell and the gate circuits [2] [3], but also appropriately designed

driver circuits. In some cases, silicon-based driver circuits featuring rise and fall times with tens of ns may limit the performance of the GaN power switches.

Regarding the characteristics of the driver circuit, not only the output resistance, but also the maximum current capability is relevant, since it significantly impacts the turn-on and -off speed of the power switch. Both parameters set the rise and fall time of the driver's output voltage (and gate-source voltage of the power switch) and thus affect switching losses.

Care should therefore be taken to ensure that the driver is not the bottleneck in terms of switching speed. Thus, both aspects, device intrinsic characteristics (output characteristics) of the driver and optimized gate layout must be addressed. Integration of the power switch and the corresponding driver circuit can mitigate the latter effect. Integration can either be implemented chip by chip or monolithically [4]. Lateral GaN-HEMTs allow for the monolithic integration of the driver in combination with the power switch [5] [6] [7] [8].

Thus, this paper presents a GaN driver to control a GaN power switch [9]. The study uses GaN-on-AlN/SiC devices fabricated on a semi-insulating SiC substrate using an AlN buffer to suppress back-gating. The same epitaxial stack and back-gating immunity enables monolithic integration in a next step. The transistors in this study are normally-on devices with an iridium (Ir) based gate contact, which forms a Schottky-diode that is forward biased for a positive gate-source voltage. The electrical characteristics at the gate are similar to gate injection transistors (GITs), as the Schottky contact at the gate has the opposite direction compared to commercial Schottky gate GaN-HEMTs. Consequently, a continuous gate

current is required to maintain the positive turn-on voltage leading to similar gate driving requirements to GITs, just with an additional negative bias for turn-off. Therefore, these results are also applicable for normally-off p-GaN gate devices with an ohmic gate contact.

The aim of the presented work is to characterize the gate driver that is implemented in GaN-technology regarding its static and dynamic characteristics. In the end, the paper shows switching operation of the GaN driver using a load emulation, which substitutes the input characteristic of a GaN power switch.

Driver Topology

This section describes the driver topology. First of all, some terms are introduced to allow clear explanations. This paper shows a characterization of a GaN driver which should control a GaN power switch. Thus, the “power switch” is a GaN-HEMT used as a switch for power electronic applications (e.g. half-bridge topology). The term “GaN driver” refers to a circuit that controls the power switch and is itself realized as a monolithic GaN chip.

The complete setup comprises three major blocks, shown in Fig. 1. The first ones are commercially available driver circuits, which receive pulse width modulation (PWM) signals and feed them into the GaN driver, which is to be studied.

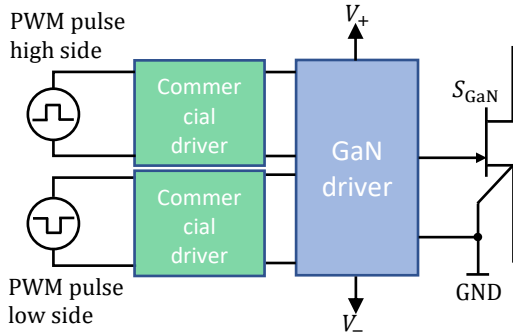


Fig. 1: Structure of gate driver test setup: commercial gate driver, GaN driver, and GaN power switch

Fig. 2 depicts the commercial driver and its auxiliary circuit to drive the gate of non-isolated GaN power switches [10] [11]. The commercial driver IC (see Fig. 2, circuitry shown for the high side transistor of the GaN driver, low side circuitry has equal structure) outputs two voltage levels: $V_{+,HS}$ and $V_{-,HS}$. $R_{on,ss,HS}$ sets the steady-state current fed into the gate of the GaN driver, whose schematic is shown in Fig. 3. $C_{s,HS}$ and $R_{on,HS}$ provides the charge to quickly bring the

gate-source voltage $v_{GS,HS}$ of the GaN driver’s transistor above the threshold voltage. This is the driving voltage of the high side transistor within the GaN driver. It is supplied by two voltages (V_+ and V_-) with the values 9 V and -4.6 V respectively.

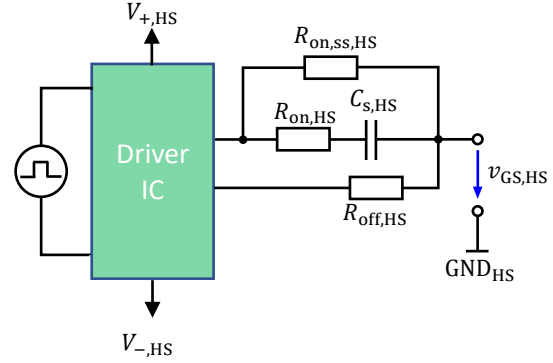


Fig. 2: Commercial gate driver with auxiliary circuit for high side switch of GaN driver

The GaN driver itself consists of several components monolithically integrated onto one single die (see Fig. 3, shaded area).

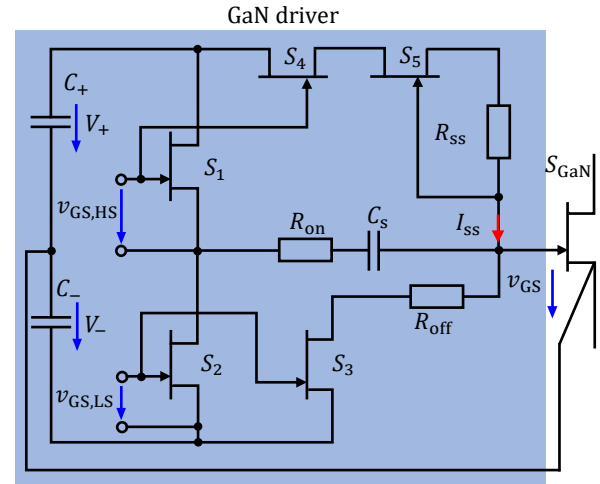


Fig. 3: Internal schematic of the driver including GaN power switch

$v_{GS,HS}$ and $v_{GS,LS}$ serve as input signals to the GaN driver (generated by the commercial driver stage shown in Fig. 2). S_1 is the high side switch to turn on the power switch S_{GaN} by the auxiliary circuit (R_{on} , C_s and a current source). S_4 , S_5 and R_{ss} form a linear current source, which supplies the steady-state current I_{ss} required by the power switch (S_{GaN} [10]). R_{off} in conjunction with S_2 and S_3 represent the turn-off current path, which can be triggered by applying a positive voltage to $v_{GS,LS}$. In order to achieve fast turn-off of the power switch, two transistors (S_2 and S_3) are used. S_2 provides a fast turn-off path with C_s and

R_{on} , while S_3 holds the power switch in off-state (steady-state). This also improves robustness against Miller-induced turn-on [12]. The capacitors C_+ , C_- and C_s (see Fig. 3) are directly placed on the die. Fig. 4 depicts a photograph of the GaN driver die placed on a submount (small PCB), with the capacitors on top. The driver is soldered onto the submount and its electrical connections are made by wire bonds. The resistors R_{on} , R_{off} and R_{ss} are directly processed within the semiconductor chip (no external components). A photo of the driver chip itself is shown in Fig. 4 (upper).

Table I: Parameters of the GaN driver

Parameter	Value	Parameter	Value
V_+	8.9 V	C_+	4.4 nF
V_-	-4.6 V	C_-	4.4 nF
I_{SS}	15 mA	R_{SS}	128 Ω
C_s	4.4 nF	R_{on}	6.5 Ω
R_{off}	3.5 Ω		

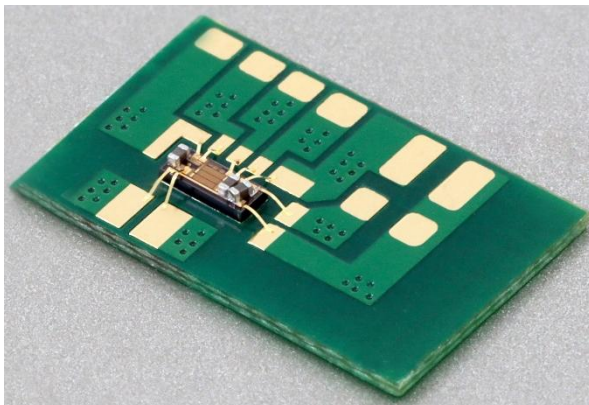
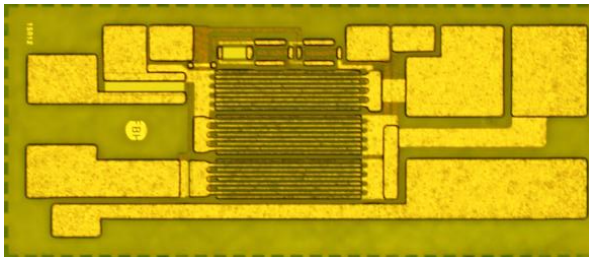


Fig. 4: Photograph of the GaN driver chip (upper) and GaN driver placed on a submount (small PCB, lower); capacitors directly soldered onto chip

In the following investigations, for characterization purposes the GaN driver is not feeding a real transistor, but an artificial load that represents the input characteristic of a power transistor. This is also typically done in driver datasheets. It is intended to monolithically

integrate the driver with a power transistor in the next steps. Fig. 5 shows the structure of the artificial load. $C_{iss,PS}$ is close to the input capacitance of the power switch [13]. The diodes of type BAV70HY model the continuous (steady-state) current of the power switch (Schottky gate). The diode is selected by comparing the input characteristics of the power switch to the diode's forward characteristic.

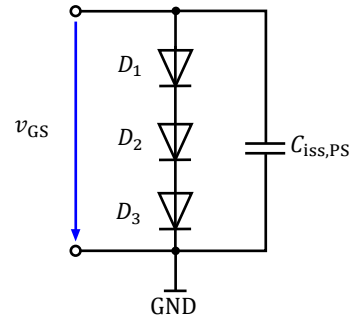


Fig. 5: Schematic of the load emulation representing the input characteristic of the GaN power switch (gate leakage and input capacitance)

Characterization of the Driver

In order to achieve fast switching, the properties of the driver must be accurately known. This allows to properly select the gate driving conditions at the driver's input in order to generate very steep edges at the output of the driver.

This section describes the characterization of the high side switch (S_1 in Fig. 3). To do so, the capacitors (C_+ , C_- and C_s from Fig. 3) are not mounted to the die (for all measurements) in order to get the characteristics of the GaN transistor within the GaN driver itself. This prevents the leakage current of the capacitors from being incorrectly attributed to the transistor. Furthermore, as C_s is removed for the measurements, no additional conductive path apart from the high side transistor S_1 itself is present within the GaN driver. The low side transistors (S_2 and S_3) are in off-state by applying a gate-source voltage of -5 V during all measurements.

Static Characterization

In case of the studied transistors, the Schottky-diode of the gate stack is forward biased if the device is turned on, leading to a current at the gate if the gate-source voltage exceeds the threshold voltage of the intrinsic diode at the gate. This behavior can be seen in Fig. 6, which depicts the gate leakage current versus gate-source voltage in

a range from -6 V up to the threshold voltage of the Schottky-diode. The curve results from a slow sweep of the gate-source voltage at a small drain-source voltage (<1 V). At a gate-source voltage of approximately 1.5 V, the Schottky-diode conducts around 1 mA. With negative gate-source voltage, the gate leakage stays below 1 μ A, as the diode at the gate is reverse biased and blocks. As can be seen from the right part of Fig. 6, a (small) constant gate current must be fed to the device to keep it in on-state.

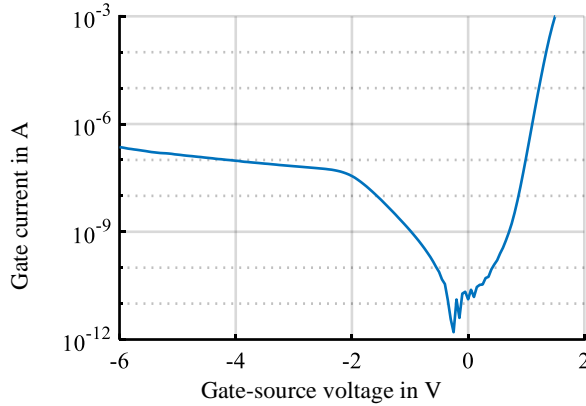


Fig. 6: Gate leakage versus gate-source voltage of the high side transistor S_1 of the GaN driver

Next, the drain leakage current is studied. It determines the breakdown voltage of the device and is characterized as a function of the drain-source voltage. In general, leakage currents within GaN are significantly higher than with SiC- or Si-MOSFETs [14]. With rising drain-source voltage, leakage also increases at a gate-source voltage of -5 V (see Fig. 7).

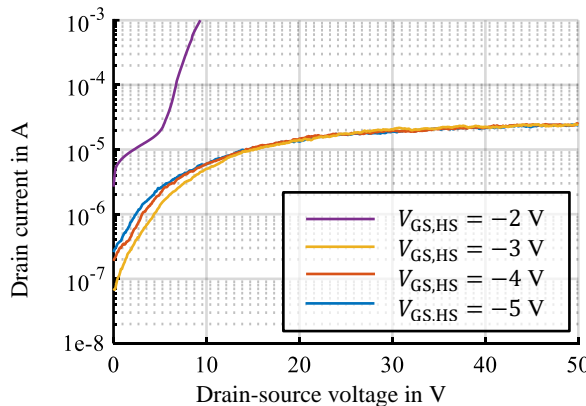


Fig. 7: Drain leakage versus drain-source voltage of the high side transistor S_1 depending on its gate-source voltage $V_{GS,HS}$ of the GaN driver at $V_{GS,LS} = -5$ V

For gate-source voltages up to -3 V, no impact of gate-source voltage on the drain current is visible. At -2 V, a significant increase can be

noticed, which is due to exceeding the transistor's threshold voltage.

The transistor's threshold voltage defines the point at which it starts to conduct significant current between the drain and source terminal. Thus, this value is needed to select gate drive conditions. Proper selection of gate-source voltage levels ensures safe operation and fast switching. Consequently, the threshold voltage and transfer characteristic of the transistor is studied. Fig. 8 depicts the transfer characteristic for different drain-source biases. First, the test setup applies the off-state gate-source voltage to the driver and then sets a specified drain bias [15]. After that, a slow sweep starts which increases the gate-source voltage by 1 mV-steps. When reaching the current at which the threshold voltage is defined (here, we use 1 mA), the sweep stops. This avoids damage to the transistor, as higher gate-source voltages would result in significantly higher drain currents and thus, power loss. For gate-source voltages far below the threshold voltage, only leakage currents of several μ A are present. As the transistor turns on between -3 V and -2 V gate-source voltage, the drain current significantly increases. For a drain bias of 5 V, a threshold voltage of -1.97 V results. With higher drain bias, its shifts to more negative voltage values (-2.14 V at 20 V drain bias).

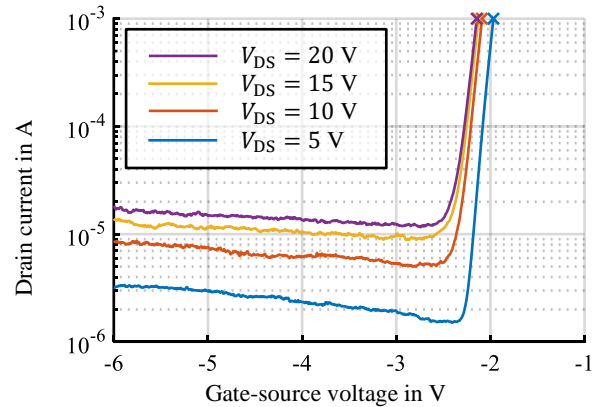


Fig. 8: Transfer characteristic for different drain-source voltages of the GaN driver

As the intrinsic capacitances primarily impact the switching transitions and switching losses, these need to be characterized as well. Typically, they are assessed by small signal measurements versus drain-source voltage. Fig. 9 depicts the input capacitance C_{ISS} , output capacitance C_{OSS} , and reverse transfer capacitance C_{RSS} for the transistor. All capacitances are in the range of several pF and drop slightly with rising drain-source voltage. The input capacitance lies slightly

below the output capacitance. Beneficially, the reverse transfer capacitance is the smallest.

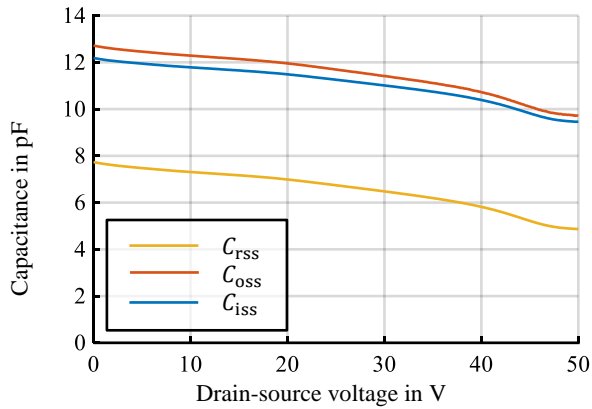


Fig. 9: Small signal capacitances versus drain-source voltage of the GaN driver at $V_{GS} = -5$ V

In order to properly select the gate drive circuit for the GaN driver, its input capacitance should also be characterized depending on the gate-source voltage. During the switching transitions, the gate-source voltage changes from the off-state voltage which is significantly lower than the threshold voltage of the device to the on-state voltage. Fig. 10 depicts how the input capacitance changes with the gate-source voltage. As can be noted from the diagram, the capacitance triples from around 10 pF to more than 30 pF when increasing the gate-source voltage from -6 V to 0 V. Above 0 V, the leakage current is so high, that measuring the input capacitance is no longer possible. This figure reveals that a higher gate charge is required to turn on the device as expected from the measurements of the input capacitance versus drain-source voltage.

Pulsed Characterization

Pulsed characterization allows for obtaining the output characteristic, transfer characteristic and on-state resistance of the transistor. In order to avoid significant self-heating of the device impacting the measurement, pulse lengths of $5 \mu s$ are used. The test setup has been introduced in [16] and pulses the drain voltage while keeping the gate-source voltage constant. Each short voltage and current pulse delivers one measurement point in the output characteristic shown in Fig. 11. For the GaN driver studied here, only the first quadrant of the output characteristic is relevant, as no negative drain current occurs during the operation. The driver charges the input capacitance of the power switch during turn-on. To do so, the high side transistor of the driver conducts and delivers a positive drain current. During the power switches' turn-

off, the low side transistor of the driver is in on-state. The driver sinks a current to discharge the input capacitance of the power switch. Thus, the low side transistor of the driver also conducts a positive drain current.

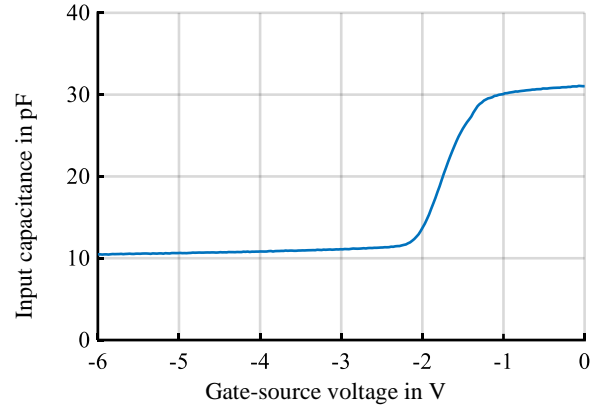


Fig. 10: Small signal input capacitance versus gate-source voltage of the GaN driver at $V_{DS} = 0$ V

By increasing the drain-source voltage, the driver exhibits an ohmic behavior and then reaches the saturation region when the gate-source voltage is higher than the threshold voltage of the device. A nearly linear rise of the saturation current is visible with a linear sweep of the gate-source voltage. At a gate-source voltage of 1 V the device is fully turned on. Higher gate-source voltages than 1 V will cause a significant gate current to flow, which is unintended. For a gate-source voltage of 1 V, a saturation current of roughly 3.5 A results.

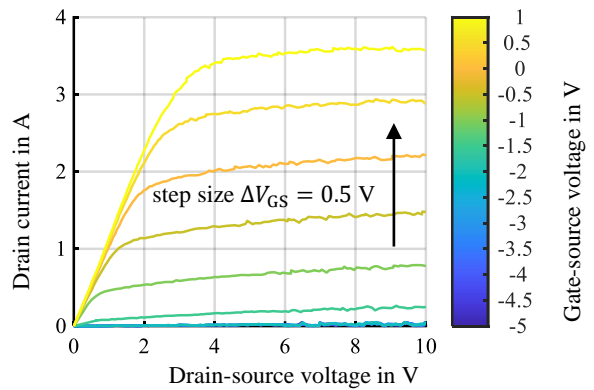


Fig. 11: Output characteristic of the GaN driver generated by pulsed (μs) measurement

From the output characteristic, also the transfer characteristic can be extracted. Fig. 12 shows the transfer characteristic extracting the data from Fig. 11 at a drain-source voltage of 5 V. Comparing the threshold voltage of around -2 V given in Fig. 12 to the static measurement in Fig. 8 gives consistent results.

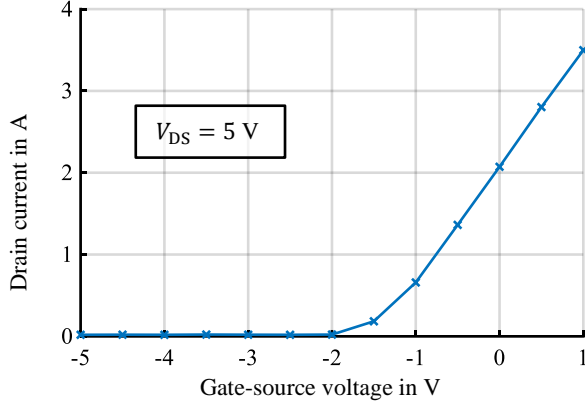


Fig. 12: Transfer characteristic of the GaN driver generated by pulsed measurement

Also, the on-state resistance can be obtained from the output characteristics using the behavior at low drain-source voltages (1...2 V). Fig. 13 shows the on-state resistance versus gate-source voltage. Fully enhanced, the driver shows an on-state resistance slightly below 1 Ω . The epitaxial stack and device processing of the GaN-on-AlN/SiC wafer is similar as for the high voltage transistors reported in [17]. These have a gate drain separation of 15.25 μm and are intended for high voltage applications and show acceptable on-state resistance increase in static on-wafer measurements. The drivers feature a gate-drain separation of 4.25 μm and operate below 15 V. Therefore, we expect minor to negligible on-state resistance increase for the drivers during operation.

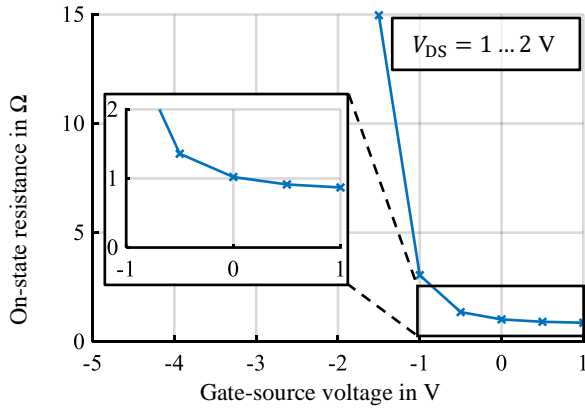


Fig. 13: On-state resistance of the GaN driver generated by pulsed measurement

According to the on-state resistance in Fig. 13 and the saturation current in Fig. 11, the on-state gate-source voltage should be chosen above 0 V. Using a gate-source voltage of +1 V gives a peak current of ≈ 3.5 A that can be delivered by the driver to transiently charge the input capacitance of the power switch. During the turn-off process of the power switch S_{GaN} , both transistors S_2 and

S_3 are turned on (see Fig. 3). This forms two discharge paths to turn off the transistor S_{GaN} . The first one is through the resistor R_{off} and S_3 and the other is given by the capacitor C_s and S_2 .

Switching operation

After finishing the static characterization, switching operation follows. For these measurements, the capacitors C_+ , C_- and C_s of the GaN driver are mounted. In order to operate the GaN driver, the component values of the circuitry (Fig. 2) of the commercial gate driver need to be selected, as these parameters significantly impact switching speed [18]. Table II summarizes the component values to drive the input of the proposed GaN driver.

Table II: Parameters for switching operation

Parameter	Value	Parameter	Value
$V_{+,HS}$	8.9 V	$V_{+,LS}$	8.9 V
$V_{-,HS}$	-4.6 V	$V_{-,LS}$	-4.6 V
$R_{\text{on,ss,HS}}$	16 k Ω	$R_{\text{on,ss,LS}}$	8.2 k Ω
$R_{\text{on,HS}}$	32 Ω	$R_{\text{on,LS}}$	27 Ω
$C_{s,HS}$	270 pF	$C_{s,LS}$	330 pF
$R_{\text{off,HS}}$	66 Ω	$R_{\text{off,LS}}$	33 Ω

Normally, the double-pulse test serves as the standard method to evaluate the switching transitions for power switches. It also allows for switching loss characterization. The GaN driver itself also consists of power transistors, which is why the characterization up to now looks like the same procedure as for a power switch [19] [20]. However, in contrast to the typical situation for power transistors, the GaN driver is loaded by the input impedance of the power switch that has a capacitive instead of an inductive behavior. Of course, the power switch exhibits ohmic capacitive behavior, but during the switching transitions, the capacitive behavior dominates. Thus, the double-pulse test using an inductive load does not reflect the situation in the application. Therefore, the double-pulse test is omitted for the characterization of the GaN driver. Instead, the paper presents continuous switching of the driver with a fixed frequency using the artificial load (Fig. 5), which emulated the input characteristic of the power switch. Operating the GaN driver in continuous operation gives the waveforms in Fig. 14 for the input signals of the driver ($v_{\text{GS,LS}}$ and $v_{\text{GS,HS}}$) as well as

the output of the driver (v_{GS}), which serves as the gate signal for the power switch (the artificial load shown in Fig. 5). In off-state, the driver outputs the negative gate supply voltage of -4.6 V, whereas in on-state, the voltage remains at around 2.2 V and does not reach the positive gate supply voltage of 8.9 V, as the driver sources a constant current of 15 mA, which generates a voltage drop of around 2.2 V at the transistor's gate.

Fig. 15 displays the rising edge of the driver's output v_{GS} as well as the inputs. The driver's output features a rise time of 1.68 ns (10 % to 90 %). From the driver's output, no distinctive Miller-plateau is visible, as it is loaded by an ohmic-capacitive load (see Fig. 5) replacing a real power switch for characterization purposes. Thus, no drain-source voltage commutation of the power switch occurs.

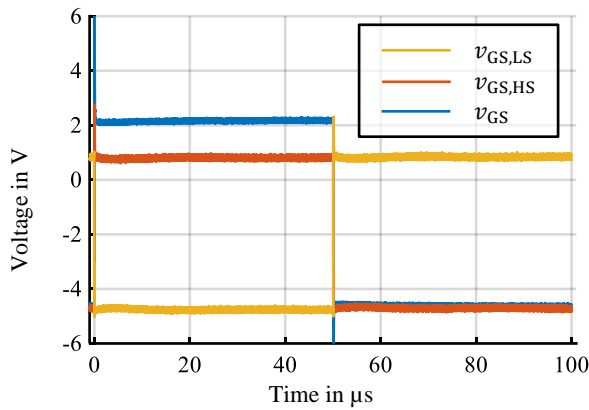


Fig. 14: Switching period of the driver: Gate-source voltage of the power switch (load emulation) and input signals of the GaN driver

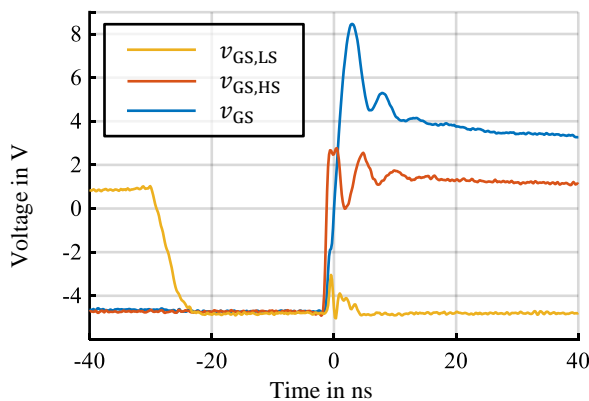


Fig. 15: Rising edge of the driver's output: Gate-source voltage of the power switch (load emulation) and input signals of the GaN driver

The falling edge of the driver output voltage is shown in Fig. 16 along with the corresponding input signals. Again, there is no distinctive

Miller-plateau (at v_{GS}) as the load is solely ohmic capacitive. The resulting fall time (90 % to 10 %) is 1.84 ns.

The transient measurements prove that the GaN driver can deliver a gate-source voltage with fast edges to enable steep switching transients of a GaN power switch.

Conclusion

This paper demonstrates a driver circuit based on lateral GaN technology to control a GaN power switch. The complete characterization is done studying the high side switch of the internal circuitry. First, static measurements of the leakage currents deliver reasonable results. The threshold voltage of the driver transistor is around -2 V. The intrinsic capacitances lie in the range of some pF, which promises fast switching transitions. From the pulsed characterization, a saturation current of 3.5 A and an on-state resistance slightly below 1Ω result. Using the complete driver in switching operation with a load emulation gives rise and fall times of 1.68 ns and 1.84 ns, respectively. Further work comprises the combination of the GaN driver with a GaN power switch before monolithically integrating both.

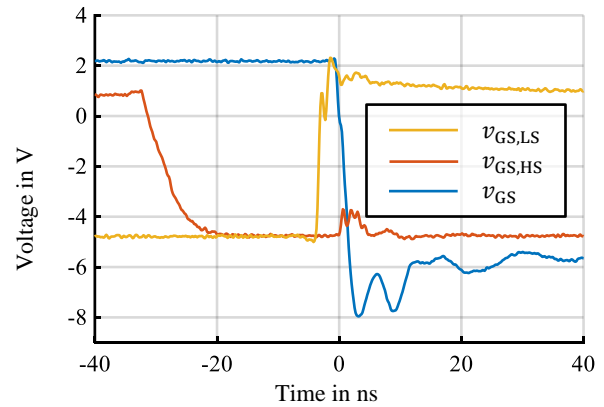


Fig. 16: Falling edge of the driver's output: Gate-source voltage of the power switch (load emulation) and input signals of the GaN driver

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