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Parasitic Capacitances Effect on Transient Current Sharing in Parallel Connection of GaN FETs

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Keywords

«Device application», « Gallium Nitride (GaN)», «Parallel operation», «Parasitic elements».

Abstract

The paper deals with the impact of parasitic capacitance on the switching operation of GaN FET devices in parallel connection. A suitable experimental board has been developed to investigate the switching transient current share features for several GaN FETs connected in parallel to perform a single high-current switch. Every device can be driven independently, and a source shunt per each GaN FET monitors the transistor current. Simulation runs and experimental tests show the switching mechanism and parameters involved in the transients' current share. The paper aims to give insights into the designing boards of paralleled GaN FETs regarding the influence of parasitic capacitances in the transient current peak distribution to find the maximum parasitic capacitance reachable without overcoming the limit of impulsive device current. The study

contributes to developing reliable power modules made of several GaN FETs in parallel connection.

Introduction

In power electronics, the use of emerging high electro-mobility devices like Gallium-Nitride (GaN) FETs is growing due to their remarkable advantages. Especially in low-voltage applications (<100 V), GaN-based power transistors are becoming popular due to their high performance compared to their silicon (Si) device counterparts [1]. To extend the current capability for applications such as inverters for mild hybrid electric vehicles or DC-DC converter [2] charging for battery energy storage systems, the parallel connection of GaN FETs can be arranged [3]. In a parallel connection, the current share shows a mismatch in switching transients as well as in on-state operation due to the differences among technology parameters such as the threshold voltage, V_{GSth} , the transconductance g_{fs} , the junction temperature T_J , the inner gate resistance, and the parasitic capacitances. Furthermore, the output electrical parameters, such as the driver gate resistance and the parasitic inductances, influence the current mismatch [4]. In the proposed paper, the current transient due to the parasitic capacitances and inductances' can be investigated. Simulation results and experimental assessments have been carried out through a specifically developed board used as a workbench performing several tests to investigate the current sharing in transient switching. A testing methodology addressed to separate the contribution of the transient current behavior of

the parasitic capacitance concerning stray inductances has been developed. The parasitic capacitances effect evaluation provides guidelines for optimizing the performance of GaN FET devices in parallel connections. The results allow us to evaluate the maximum peak transient current at power-on relative to the parasitic capacitances caused by the devices and the board's layout. The pulse peak current must not exceed the limits of a single device in terms of value and duration described in the GaN FET datasheets. The dynamic sharing of the drain current is focused on considering the parameters spread impact, the gate driver influence, and the effective layout solutions.

Testing methodology

The methodology for analyzing the contribution of parasitic capacitances is based on a suitable gate control strategy acting on a programmable delay for each device. For this purpose, an experimental electronic board was developed with several devices in parallel (up to 12 low-voltage GaN FETs), in which every component is driven by its gate driver circuit. For each device, the source current can be evaluated through a resistive shunt. The tests are carried out considering the paralleled devices, (EPC2032 from EPC manufacturer, $V_{DSmax}=100V$, $I_D=101A$ at $25^\circ C$, pulse current $I_{Dpulse}=408A$ for $300\mu s$ at $25^\circ C$) supplying an inductive load ($L_{load}=90\text{ nH}$) and a freewheeling super-fast diode, as illustrated in the schematic circuit model of Fig. 1.

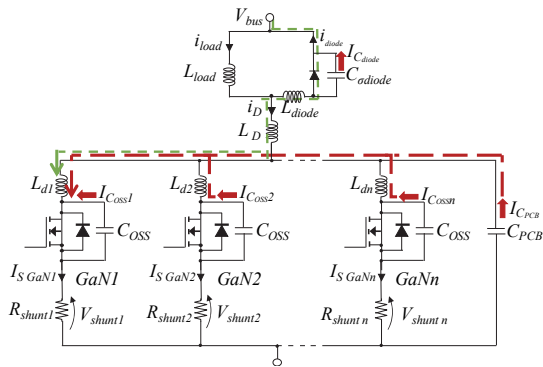


Fig. 1: Electrical schematic of the system used for the test with the equivalent electrical model of the board with GaN FETs connected in parallel.

The PCB equivalent parasitic capacitance board (C_{PCB}) and GaN FETs output capacitances (C_{OSS}) is also reported. The DC input voltage is fixed at $24V$. In the tests, GaN FETs are driven with a switching frequency of 100 kHz and duty cycle

$d=0.5$. $C_{oss} = C_{DS} + C_{GD}$ represents the non-linear output capacitance of a single GaN FET [5]. The C_{PCB} is related to the layout of the board as described in the next subsection. The inductances arrangement in Fig.1 is essential in the test method presented. L_{diode} is the parasitic inductance of the diode (in this case $L_{diode}=20\text{ nH}$). L_d represents the inductance that interconnects the GaN FETs with each other (in this case is estimated at 2.7 nH). L_D is the inductance that connects the board's drain to the load. It has been designed to be 20 times larger than L_d . This design choice allows to observe the contribution at turn-on of the load inductive current and the discharge currents of the global parasitic capacitances in the transient current peak. To understand better this procedure, several simulation tests (in LTSpice software with a developed GaN FET model [6]) at turn-on are carried out considering $n=8$ devices in parallel connection. Only one GaN FET (GaN1) is activated while the remaining $n-1$ are kept off-state (the worst case for the current flowing in the device turned on). The simulations are repeated for various values of $L_{diode} + L_D$: 0.1% , 1% , 10% , 50% , and 100% concerning the actual value of the PCB design considered. An ideal LTSpice diode in antiparallel of load inductance is considered for the sake of simplicity to focus on the GaN FET performance during the transient operations, without introducing current and voltage oscillations during transients, due to the real diode parasitic components. In Fig. 2a, the top section displays waveforms of the board drain-source voltage (V_{DS}), load current (I_{load}), and the current in the board drain (I_D).

In the lower section of Fig.2a, the waveforms of the current conducted by GaN FET1 (I_{SGaN1}), and by GaNFET,n ($I_{SGaN,n}$), are shown. In Fig 2a the current peak I_{SGaN1} is due to the effect of the V_{DS} fall at GaN FET1 turn-on with the parallel parasitic capacitances (see Fig. 1).

Furthermore, the current peak is affected by the load current rising. At the growth of $L_D + L_{diode}$, the current slope decreases, and the current peak is affected only by the global parasitic capacitances as shown in Fig. 2b, where the I_{SGaN1} peak remains constant at I_D amplitude variation. Therefore, as displayed in Fig. 2b with large drain inductances the effects on currents caused by the discharge of parasitic capacitances and the rise of drain current are decoupled. The current peak due to the parasitic capacitances of N_{GaN} used can be estimated as

$$I_{Ctot\ peak} = C_{tot} \cdot \frac{V_{DC}}{\Delta t} = (C_{PCB} + N_{GaN} \cdot C_{OSS}) \cdot \frac{V_{DC}}{\Delta t} \quad (1)$$

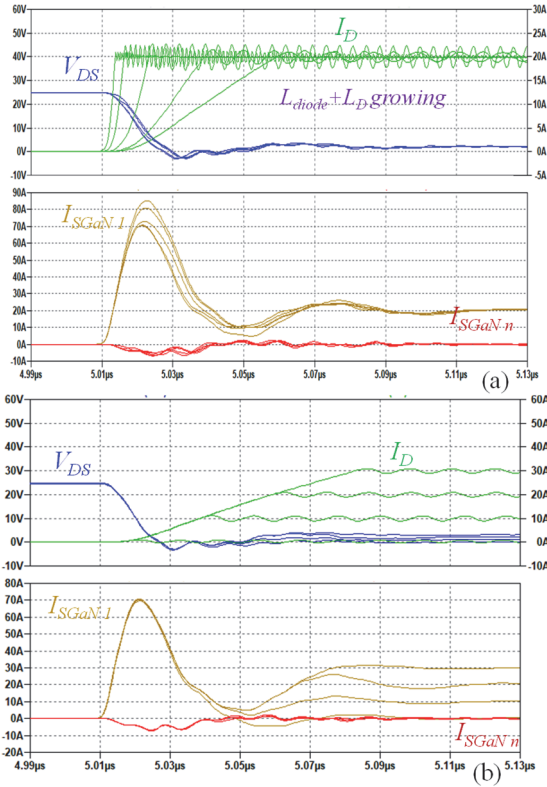


Fig. 2: Simulation results a) Turn-on transient at $I_D=20$ A, only GaN FET1 is turned on. Waveforms of V_{DS} , I_D , I_{SGaN1} , I_{SGaNn} for different $L_D + L_{diode}$: 0.1% 1% 10% 50% and 100% of the actual drain inductance ($L_D + L_{diode}=50\mu H$). Time =20 ns/div. b) turn on the current peak of GaN FET1 at different drain currents at low di/dt .

With this fundamental achievement is possible to investigate the turn-on current sharing due to the effect of parasitic capacitances.

The experimental test board developed for the parallel connection operation

The parallel GaN FETs test board for a high current switch (up to 200 A) composed of 12 parallel connected GaN FETs (EPC2302 from Efficient Power Conversion) distributed in two rows used as a workbench for the experimental evaluation is shown in Fig. 3. The board features two driver options— a common PWM gate driver for all devices and a single gate driver for each GaN FET. A shunt resistor $R_{shunt}=0.1 \Omega$ in the source path, out of the gate loop, is used for the current sense.

The equivalent capacitance C_{PCB} evaluation procedure

The C_{PCB} is related to the layout of the developed circuit board. The portion of the board considered consists of 14 internal layers with a thickness of 2 oz. Each layer is electrically connected to one net between the GaN FETs' drains, GaN FETs' sources or the board's sources, in an alternate sequence. Overall area of the board is $A=135 \text{ cm}^2$. Consequently, the equivalent capacitance between two layers connected to different nets of the board x and y can be calculated as

$$C_{xy} = D_{xy}/(\epsilon_0 \cdot \epsilon_r \cdot A) \quad (2)$$

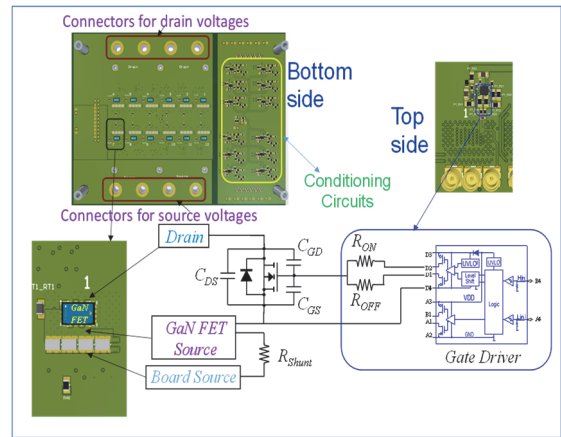


Fig. 3: Test board for GaN FETs in parallel connection

All the switching waveforms are carried out at ambient temperature (27°C) at V_{Load} equal to 24V.

where ϵ_0 is the vacuum permittivity; $\epsilon_r=3.7$ is the relative permittivity of the dielectric; D_{xy} is the distance between the layers x and y minus the thickness of the layer conductors [7]. For the drain (D), device source (FS) and board source (BS) layers. Between the device source and the board source there is the shunt resistance (the gate driver circuit is referred to the device source as described in Fig. 3). The distance D_{xy} is different when considering the case with layer x immediately below layer y (consecutive), or the case where layer x and layer y present a third layer of a different net in the between (non-consecutive). In Fig. 4 the parasitic capacitances model adopted for the actual experimental board schematic is described.

Furthermore, in Fig.4 the parasitic capacitance of an equivalent three layers parasitic capacitances are highlighted, in which the consecutive

capacitance are $C_{BS,FS}$ (between BF and FS) and $C_{FS,D}$ (between FS and D), while $C_{BS,D}$ (between BF and FS) is a parasitic capacitance between two non-consecutive layers (the values of the computed capacitances $C_{BS,FS}$, $C_{FS,D}$ and $C_{BS,D}$ are described).

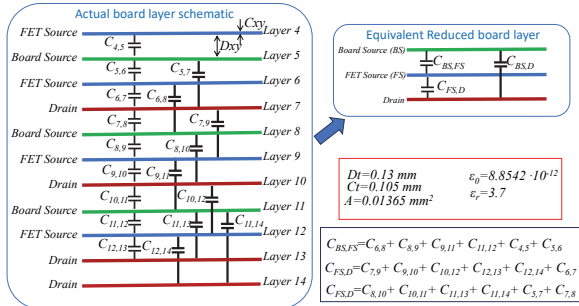


Fig. 4: Parasitic capacitances schematic model of the experimental test board.

Considering consecutive layers, the distance is $D_{xy}=0.13$ mm and results to $C_{xy}=3.415$ nF, while $D_{xy}=0.365$ mm and $C_{xy}=1.216$ mm are obtained for non-consecutive layers.

Capacitances connected between the same two layers (drain- device source D,FS; drain-board source D,BS; device source-board source FS,BS) are connected in parallel. The equivalent capacitances between the layers are $C_{FS,BS}=16.1$ nF; $C_{D,FS}=13.9$ nF; $C_{FS,BS}=11.2$ nF.

Parasitic capacitances effect at turn-on switching transients

The designed test board is used considering 8 GaN FETs in parallel connection and the freewheeling super-fast diode (APT40DQ60BG) in antiparallel of load inductance. The number of device used influence the equivalent capacitance C_{oss} as described in Fig.1. For focusing the effect of the equivalent capacitance, the test is performed driving two GaN FETs between the 8 with six devices in the turn-off state. The six devices influence the current transient through their output capacitances charge contribute. The purpose of the test is to show the effect in the GaN FET transient current of the parasitic capacitances when they are in parallel connection and driven with a time mismatch. The time mismatch between the GaN FETs represents the effects of a different gate loop inductance or the spread of dynamic parameters, such as the threshold voltage [8]. In the experimental test the delay is obtained acting on the driving signals V_q .

Fig.5a shows the electrical schematic relative to GaN1 and GaN2 in parallel connection driven with V_{q2} in a delay of Δt_{delay} respect of V_{q1} . The resulting waveforms of the drain-source voltage V_{DS} and the board drain current I_D are depicted in blue and in green respectively in all experimental results. Additionally, Fig. 5 shows the measured currents of GaN1 I_{S1} (yellow), GaN2 I_{S2} (red), and the one of a generic not driven GaN8 I_{S8} (magenta). The transient current is evenly distributed between the two devices. If a turn-on delay on GaN2 compared to GaN1 is introduced, the device that turns on first has a peak much higher than the second, relating to the length of the delay. Results obtained without delay are reported in Fig.5b, while the waveforms achieved with $\Delta t_{delay}=5$ ns and $\Delta t_{delay}=9$ ns are depicted in Fig.5c and Fig.5d, respectively.

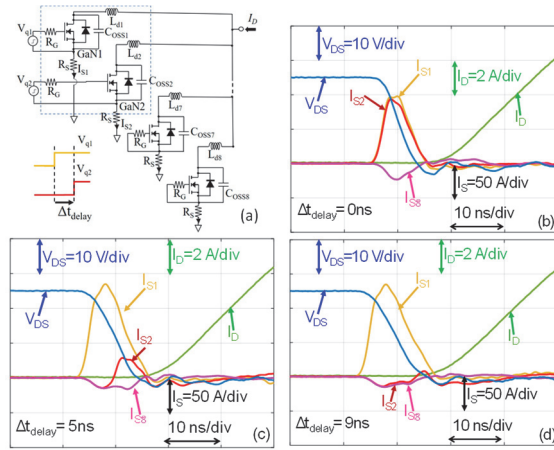


Fig. 5: Turn-on transient driving GaN2 with a delay in respect of GaN1. a) electrical schematic of the two GaN FETs in the board driven with time-delayed V_q . b) delay=0 ns. c) delay=5 ns. d) delay=9 ns. $I_S=50$ A/div. $I_D=2$ A/div. $V_{DS}=10$ V/div. Time $t=10$ ns/div.

Comparing Fig.5b, Fig.5c and Fig.5d, the I_D waveform is unchanged. Looking at Fig.5a, during the V_{DS} fall, I_{S1} and I_{S2} have a current peak due to the parasitic capacitances contribution. These peaks are congruent because of the simultaneous turn-on. The total charge of the parasitic capacitances is split equally between GaN1 and GaN2. Introducing a $\Delta t_{delay}=5$ ns in Fig.5c, I_{S1} peak is higher than I_{S2} because GaN1 is the only GaN FET that conducts all the capacitive current until GaN2 is turned on. Immediately after the GaN2 turn-on, the capacitive current is conducted by the two devices with different I_S . In the case of $\Delta t_{delay}=9$ ns in Fig.5d, the Δt_{delay} is long as the V_{DS} variation and

GaN2 turn on in zero voltage switching (ZVS) without contributing to the capacitive current conduction [9]. In this case, I_{S1} peak is maximum and I_{S2} acts as I_{S8} (as all the devices in off state). Furthermore, Fig.5 shows that V_{DS} fall and the transitory turn-on duration appear longer in Fig.5c and Fig.5d than Fig.5b, as the Δt_{delay} is longer.

Overall, the delay between V_{q1} and V_{q2} lead to higher peak currents in I_{S1} , directly correlated with the variations in V_{DS} . The I_D current does not impact I_S because of the slow rise due to the high L_D of the PCB. This experimental setup highlights the importance of managing turn-on delays to control peak currents and reduce associated losses in GaN FET applications.

Parasitic capacitances effect at turn-off switching transients

The experimental tests are extended at turn-off with the same methodology approach.

Fig. 6a illustrates the electrical schematic of GaN1 and GaN2 connected in parallel, with V_{q2} delayed by Δt_{delay} relative to V_{q1} . The corresponding waveforms for the drain-source voltage V_{DS} and the board drain current I_D are shown in blue and green, respectively. Furthermore, Fig. 6 presents the measured currents of GaN1 I_{S1} (yellow), GaN2 I_{S2} (red), and a generic non-driven GaN FET current I_{S8} (magenta).

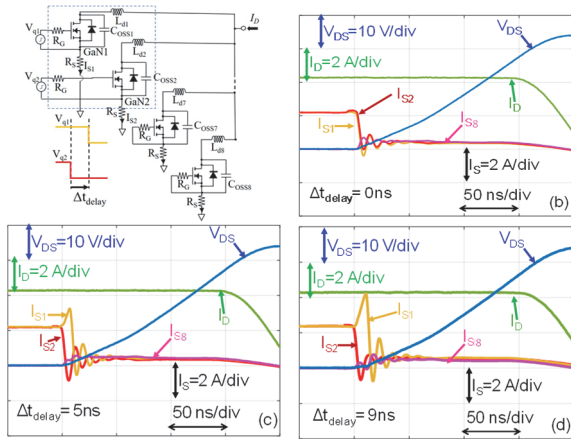


Fig. 6: Turn-off transient driving GaN2 with a delay in respect of GaN1. a) electrical schematic of the two GaN FETs in the board driven with time-delayed V_{q1} . b) delay=0 ns. c) delay=5 ns. d) delay=9 ns. $I_S=2$ A/div. $I_D=2$ A/div. $V_{DS}=10$ V/div. Time =10 ns/div

The results without delay are depicted in Fig. 6b, whereas waveforms with $\Delta t_{\text{delay}}=5$ ns and $\Delta t_{\text{delay}}=9$ ns are shown in Fig. 6c and Fig. 6d, respectively. A comparative analysis of Fig. 6b, Fig. 6c, and Fig. 6d reveals that the I_D and V_{DS} waveform remains unchanged across different delay cases. I_D falls slowly following the V_{DS} rising because of the high value of L_D . In the case without delay in Fig.6b, the turn-off of GaN1 and GaN2 occurs simultaneously due to the immediate turn-off of both FETs. This results in an equal distribution of the load current between GaN1 and GaN2 and the absence of a current peak. Introducing a $\Delta t_{\text{delay}}=5$ ns, as illustrated in Fig. 6c, results in a higher I_{S1} peak compared to I_{S2} , since GaN1 continues to conduct the entire load current alone immediately after the GaN2 turn-off. In the scenario of $\Delta t_{\text{delay}}=5$ ns depicted in Fig. 6d, the delay is long enough to leave GaN1 to conduct all the load current alone until it turns off. Consequently, at turn-off, the maximum I_S peak value corresponds to the load current, without contributions of parasitic capacitances [10]. As a result, also the delay in the turn-off has to be maintained short in order to control the maximum peak current. Nevertheless, the turn-off transient is less problematic than the turn-on.

Energy losses evaluation during switching transients

The characterization and understanding of the dynamic behavior of GaN FETs connected in parallel is crucial in high-power and high-frequency applications. Imbalanced current sharing results in increased losses and potential thermal runaway if not properly managed. By analyzing the turn-on and turn-off delays, and their corresponding energy losses [11], is essential to provide insights that can help in designing more efficient parallel GaN FET systems, ensuring better performance and longevity of the devices.

The GaN FET energy losses resulting from the experimental tests with different turn-on and turn-off delays are calculated as

$$E_{GaN} = \int_0^{\Delta t} I_S \cdot V_{DS} dt \quad (3)$$

where Δt is the time interval defined for the turn-on or the turn-off:

- turn-on: Δt it the time duration of the I_{S1} peak;

• turn-off: Δt goes from when I_{s2} starts falling and finishes when the peak of I_{s1} is elapsed. The calculated energy indicates the contribution of the parasitic capacitances and the turn-on and turn-off delay between GaN FETs connected in parallel [12].

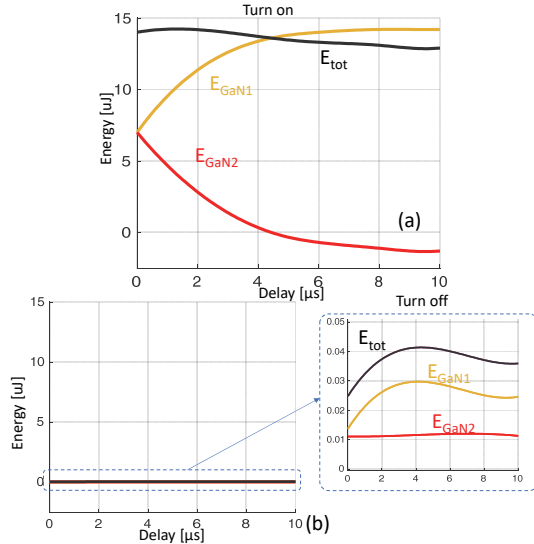


Fig. 7: Energy losses of GaN1(E_{GaN1}), GaN2(E_{GaN2}) and the sum of both (E_{tot}) obtained as a function of the driving delay. a) turn-on. b) turn-off.

The design of the PCB considered allows the contribution of losses due to load current to be excluded (the effects on currents caused by the discharge of parasitic capacitances and the rise of drain current are decoupled as discussed in the testing methodology section). Fig.7a depicts the GaN FET energies obtained with various driving delays between V_{q1} and V_{q2} at turn-on, while Fig.8b shows the results relative to the turn-off. The energy losses for GaN1 (E_{GaN1}) and those of GaN2 (E_{GaN2}) are represented in yellow and red, respectively, additionally, the sum of the two losses E_{tot} is depicted in black.

$$E_{tot} = E_{GaN1} + E_{GaN2} \quad (4)$$

Comparing Fig.7a and Fig.8b is notable that turn-on energy losses are significantly higher than turn-off losses. observation can be attributed to the major contribution of the capacitive current at turn-on. Focusing at turn-on in Fig.7a it is evident that when GaN FETs turn on simultaneously (delay is null), losses are equal for both devices. Introducing a delay in GaN2 results in higher losses in GaN1, while E_{GaN2} is reduced. In particular, a delay of 5 ns is the condition in which GaN2 exhibits $E_{GaN2}=0$ J. For delays longer than

5 ns, the negative E_{GaN2} indicates that the C_{OSS} charge of GaN2 is mostly conducted by GaN1. E_{GaN2} stabilizes to a minimum value for a Delay higher than 9 ns because all the C_{OSS} charge of GaN2 is conducted by GaN1. As a consequence, E_{GaN1} stabilizes to a maximum value for a delay higher than 9 ns. In this condition, GaN1 conducts the total parasitic current of the PCB and the parallel-connected devices. The total energy E_{tot} remains almost constant regardless of the delay since the total energy of the system is determined by the total charge and the applied voltage. The enlarged view of Fig.7b reveals that the turn-off losses of GaN1 (E_{GaN1}) and GaN2 (E_{GaN2}) are identical at 0 ns of delay due to the simultaneous turn-off of devices. A non-zero delay causes an increase in E_{GaN1} , while E_{GaN2} remains unchanged [13]. The total energy E_{tot} is at a minimum when the delay is null and increases the longer the delay time.

Conclusion

This paper has comprehensively investigated the parallel connection of Gallium-Nitride (GaN) FET devices for high-current switch applications. The key parameters influencing both the static and dynamic current sharing among paralleled GaN FETs were analyzed, with a particular focus on the parasitic capacitances and the parametric spread causing non-simultaneous switching. Precise layout management and gate driver design allow to minimization of current imbalances and peak currents during switching transients.

Through detailed simulations and experimental validations, it was demonstrated that parasitic capacitances and inductances significantly impact the current peaks during switching events. Furthermore, the energy losses related to the effect of the parasitic capacitance are evaluated. Tests on a prototype board with 8 low-voltage GaN FETs connected in parallel have highlighted the importance of managing turn-on delays to control peak currents and reduce associated losses. Findings suggest that simultaneous turn-on of devices minimizes losses, while delays lead to unequal current sharing and increased peak currents in individual devices.

To minimize parasitic capacitances in PCB design, it is crucial to avoid having areas at different voltage potentials extend across the entire surface of one or more layers. Similarly, layers at different voltage potentials should not be aligned directly one above the other. A

recommended strategy is to partition each layer into multiple regions (e.g., drain, source, and common source), ensuring that regions with the same voltage potential in different layers are aligned vertically. This approach reduces the equivalent capacitance of the PCB, thereby decreasing the charge contributing to turn-on current spikes during device switching. However, the reduced equivalent capacitance leads to a faster voltage variation (dV/dt), which can increase the GaN FET peak current during turn-on events.

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